Docket No.: 1999P2198

CERTIFICATION

I, the below named translator, hereby declare that: my name and post office address are as stated below; that I am knowledgeable in the English and German languages, and that I believe that the attached text is a true and complete translation of German Application No. 199 30 118.2, filed June 30, 1999.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Description

Arrangement having a first amplifier and a second amplifier, of which in each case only one at most is intended to effect amplification

The present invention relates to a device according to the preamble of claim 1, i.e., a configuration with a first amplifier and a second amplifier, of which in each case only one is intended to effect amplification.

In existing arrangements of this type, the changeover from the first amplifier to the second amplifier, or vice versa is effected using a changeover device of greater or lesser complexity. Occasionally, such a changeover device has a relatively complicated construction and, moreover, requires at least one additional (control) terminal, which may be disadvantageous in particular in the case of integrated circuits or when accommodating the arrangement in a miniature housing; in particular, the required chip area and the RF properties may be adversely affected as a result.

The present invention is based on the object of developing the arrangement according to the preamble of claim 1 in such a way that it is possible to effect the changeover between the amplifiers with minimal additional outlay and without any disturbances.

This object is achieved according to the invention by means of a device in accordance with the features of patent claim 1.

It is provided that the second amplifier is operated depending on the conditions established at the input terminal of the first amplifier.

If the conditions depending on which the second amplifier is operated are considered to be only those conditions which do not exhibit any interactions with the signals that are to be amplified by the first amplifier, that is to say, for example, the DC voltage established at the input terminal of the first amplifier, if the signal to be amplified is an RF signal, then the changeover between the amplifiers can be controlled via the input terminal of the first amplifier. Such a changeover can be realized extremely simply and, precisely because of this simplicity, can be effected without any problems and without any effects, or at any rate without any appreciable effects, on the function and mode of operation of the amplifiers.

Advantageous developments of the invention can be gathered from the subclaims, the description below and the figure.

The invention is explained in more detail below using an exemplary embodiment with reference to the figure.

The figure shows the arrangement described in more detail below.

The arrangement described below is part of an integrated circuit. Although the advantages which can be obtained by the arrangement described are particularly great in this case, there is no restriction thereto.

The arrangement considered contains two amplifiers, of which in each case only ever one is intended to effect amplification.

In the example considered, the amplifiers are formed by a first transistor T1 and a second transistor T2. The transistors are dual-gate MOSFETs in the example considered.

At this early juncture it shall be pointed out that the amplifiers can also be formed by any other devices comprising transistors or other elements or a plurality of transistors or elements.

The transistors T1 and T2 each have a source terminal S, a drain terminal D, a first gate terminal G1, and a second gate terminal G2, the first gate terminals G1 in each case serving for the inputting of the signals to be amplified, and the second gate terminals G2 serving for regulating the gain.

The arrangement shown has external input and/or output terminals A1, A2, E1, E2, and 0. Of these terminals,

- the terminal E1 serves for inputting the signal that is to be amplified by the first transistor T1, and for controlling the changeover between the transistors T1 and T2,

- the terminal E2 serves for inputting the signal that is to be amplified by the second transistor T2,

- the terminal A1 serves for inputting a supply voltage that is applied inter alia to the drain terminal of the first transistor T1, and for outputting the signal amplified by the first transistor T1,

- the terminal A2 serves for inputting a supply voltage that is applied inter alia to the drain terminal of the second transistor T2, and for outputting the signal amplified by the second transistor T2,

- the terminal G2 serves for inputting a control voltage that is applied to the second gate terminals G2 of the transistors T1 and T2 and serves for gain setting, and

- the terminal 0 serves for inputting the ground potential that is applied inter alia to the source terminals S of the transistors T1 and T2.

The remaining components of the arrangement shown in the figure, i.e. transistors H1, H2 and S1 and resistors R_{H1}, R_{H2}, R_{E1a}, R_{E1b}, R_{E2a} and R_{E2b}, serve inter alia (but not exclusively) for putting the transistors T1 and T2,

- through suitable operating-point setting, into a state in which signals applied to the first gate terminal G1 of the relevant transistors are (can be) amplified, or,

- through suitable operating-point adjustment, into a state in which signals applied to the first gate terminal G1 of the relevant transistors are not (cannot be) amplified.

In the example considered, the operating-point setting or the operating-point adjustment is realized by virtue of the fact that DC voltages are applied to the first gate terminals G1 of the transistors T1 and T2, the level of which DC voltages is variable.

The fact that, in particular when the signals to be amplified are analog AC voltages, the operating point of the relevant

transistor is adjustable or variable by the application of a DC voltage to the gate terminal of said transistor is known and needs no further explanation.

The signals to be amplified by the transistors T1 and T2 are radiofrequency signals in the example considered. However, at this early juncture it shall be pointed out that this need not necessarily be the case.

As has already been mentioned above, the signals to be amplified are input via the terminals E1 and E2, respectively. They are conducted via capacitors (not shown in the figure) connected upstream of the terminals E1 and E2, in order to remove a direct-current component that may be present.

The signals to be amplified which are input via the terminal E1 are fed to the first gate terminal G1 of the first transistor T1. In order that these signals are optimally amplified by the transistor T1, the latter must be set to a suitable operating point by the application of a predetermined DC voltage to the first gate terminal G1. In the example considered, the DC voltage required for this purpose (for example 1.5 V) is generated internally within the relevant arrangement using the resistors R_{H1}, R_{E1a} and R_{E1b} and the transistor H1 from the supply voltage applied to the drain terminal D of the first transistor T1 and is fed to the first gate terminal G1 of the transistor T1.

If the DC voltage present at the gate terminal G1 of the first transistor T1 deviates from the ideal value (for example said 1.5 V), the transistor T1 firstly "only" no longer optimally amplifies the RF signal fed to it, and finally (for example in the case of DC voltages below 0.5 V) no longer amplifies it at all.

The signals to be amplified which are input via the terminal E2 are fed to the first gate terminal G1 of the second transistor T2. In order that these signals are optimally amplified by the transistor T2, the latter must also be set to a suitable operating point by the application of a predetermined DC voltage to the first gate terminal G1. In the example considered, the DC voltage required for this purpose (for example 1.5 V) is generated internally within the relevant arrangement using the resistors R_{H2}, R_{E2a} and R_{E2b} and the transistor H2 from the supply voltage applied to the drain terminal D of the first transistor T2 and is fed to the first gate terminal G1 of the transistor T2.

If the DC voltage present at the gate terminal G1 of the second transistor T2 deviates from the ideal value (for example said 1.5 V), the transistor T2 firstly "only" no longer optimally amplifies the RF signal fed to it, and finally (for example in the case of DC voltages below 0.5 V) no longer amplifies it at all.

In the arrangement considered, the transistor S1, in particular, ensures that only either the transistor T1 or the transistor T2 amplifies the signals fed thereto. This is achieved by virtue of the fact

- that, when a DC voltage is present at the first gate terminal G1 of the first transistor T1, which voltage enables the first transistor T1 to amplify signals input via the terminal E1, the DC voltage present at the first gate terminal G1 of the second transistor T2 is brought to a value which has the effect that it cannot amplify the signals input via the terminal E2, or

- that, when the DC voltage present at the first gate terminal G1 of the first transistor T1 is brought to a value which has the effect that it cannot amplify the signals input via the terminal E1, the DC voltage present at the first gate terminal G1 of the second transistor T2 is left at the value which enables the second transistor T2 to amplify signals input via the terminal E2.

The gate terminal G of the transistor S1, via which this is realized, is connected to the first gate terminal G1 of the first transistor T1 via the resistors R_{E1a} and R_{S1}. As a result, the DC voltage present at the first gate terminal G1 of the first transistor T1 is also present at the gate terminal of the transistor S1. This does not apply to the RF signals input via the terminal E1; these signals cannot pass through the resistors R_{E1a} and R_{S1}.

The transistor S1 is configured, then, in such a way

- that it is put into the on state by the DC voltage which must be established at the first gate terminal G1 of the transistor T1 in order to amplify the signals input via the terminal E1, and

- that it is put into the off state by the DC voltage at which the transistor no longer amplifies the signals input via the terminal E1.

If and as long as the transistor S1 is in the on state, the first gate terminal G1 of the second transistor T2 is connected to the ground terminal 0 via the resistor R_{E2a} and the transistor S1. As a result, the DC voltage established at the first gate terminal of the second transistor T2 falls to a value which has the consequence that signals input via the

terminal E2 are not amplified (cannot be amplified) by the transistor T2.

If and as long as the transistor S1 is in the off state, the DC voltage, generated from the supply voltage input via the terminal A2, at the first gate terminal G1 of the second transistor T2 maintains its value unchanged, as a result of which the transistor T2 is able to amplify signals input via the terminal E2.

In order that the DC voltage present at the first gate terminal G1 of the first transistor T1 is brought to a value which has the consequence that the first transistor T1 no longer amplifies signals input via the terminal E1 (can no longer amplify said signals on account of the associated operating-point adjustment), the terminal E1 is pulled to ground potential in direct-current terms via a switch or in any other desired way. As a result, the DC voltage established at the first gate terminal G1 of the first transistor T1 falls to a value which has the consequence that signals input via the terminal E1 are not amplified (cannot be amplified) by the transistor T1, and that the transistor S2 turns off.

In the manner described, without the provision of a dedicated changeover terminal, it is possible to achieve the situation in which, of the transistors T1 and T2, only ever one is in a state in which it amplifies applied signals.

The possibility of dispensing with a dedicated changeover terminal enables the arrangement to be realized with a minimal outlay. At the same time, the amplifiers are not disturbed in any way whatsoever.

For the sake of completeness, it shall be noted that the dual function of the terminals A1 and A2 (feeding in of the supply voltage and outputting of the amplified signals) does not pose any problems. The supply voltages are DC voltages which are fed to the terminals A1 and A2 via coils (not shown in the figure) connected upstream thereof. By contrast, the amplified signals are RF signals which are tapped off between the terminals A1 and A2 and the coils connected upstream thereof and are coupled out (preferably via a capacitor). The supply voltages and the amplified signals do not influence one another and can be isolated from one another without any problems.

Furthermore, it shall be pointed out that the arrangement described undoubtedly does not represent the only possibility for realizing the principle underlying the changeover described. This should be apparent and does not require verification by examples.

With regard to the arrangement considered in the present case, it should be noted

- that the DC voltages present at the first gate terminals of the transistors T1 and T2 may also originally have values at which the transistors T1 and T2 are unable to amplify the signals to be amplified, and/or that the DC voltages which have to be applied to the first gate terminals of the transistors T1 and T2 in order to enable them to amplify the signals to be amplified can also be input via the terminal E1 or be generated by the transistor S1 or in some other way and/or be switched through to the relevant gate terminal,

- that it is not necessarily the level of the DC voltage established at the first gate terminal of the first transistor

that has to be decisive for the operation of the second transistor, rather, in addition or as an alternative, it is also possible to take account of other conditions (for example the time profile and/or the frequency of the voltage present at the first gate terminal of the first transistor T1),

- that, instead of the resistors R_{H1} and R_{H2} and the transistors H1 and H2, it is also possible to use other ways of impressing currents (current mirroring is effected at the transistors H1 and H2 connected downstream of the resistors R_{H1} and R_{H2}), and

- that the resistors R_{E1a}, R_{E2a} and R_{S1} can also assume the value 0 Ω if $R_{E1a} << (R_{E1b} + R_{H1})$ is satisfied.

Independently of this, provision may also be made for enabling the DC voltages at the gate terminals of the transistors T1 and T2 to be altered, in addition or as an alternative, depending on voltages or signals input via other terminals from among those present (for example depending on a voltage input via the terminal G2) and/or depending on internal signals and/or depending on logic combinations of internal and/or external signals.

The arrangement described makes it possible, independently of the details of the practical realization, that the changeover between the amplifiers (formed by the transistors T1 and T2 in the present case) can be effected with minimal outlay and without disturbing these amplifiers.

Patent claims

1. An arrangement having a first amplifier (T1) and a second amplifier (T2), only one of which at most is to amplify, characterized in that
the second amplifier (T2) is operated in dependence on the ratios at the input terminal (G1) of the first amplifier (T1).

2. The arrangement as claimed in claim 1, characterized in that the conditions depending on which the second amplifier (T2) is operated are the level or the profile of the voltage established at the input terminal (G1) of the first amplifier (T1).

3. The arrangement as claimed in claim 1 or 2, characterized in that the signals to be amplified by the amplifiers (T1, T2) are analog AC voltages, and in that the conditions depending on which the second amplifier (T2) is operated are the level of the DC voltage established at the input terminal (G1) of the first amplifier (T1).

4. The arrangement as claimed in claim 3, characterized in that the DC voltage established at the input terminal (G1) of the second amplifier (T2) is varied depending on the DC voltage established at the input terminal (G1) of the first amplifier (T1).

5. The arrangement as claimed in one of the preceding claims, characterized in that the DC voltages are generated within the arrangement and applied to the input terminals (G1) of the amplifiers (T1, T2).

6. The arrangement as claimed in claim 5, characterized in that the DC voltages which are generated internally and

applied to the input terminals (G1) of the amplifiers (T1, T2) have a value which enables the amplifiers (T1, T2) to amplify the signals to be amplified.

7. The arrangement as claimed in one of claims 3 to 6, characterized in that when the DC voltage established at the input terminal (G1) of the first amplifier (T1) has a value at which the signals that are to be amplified by the first amplifier (T1) can be amplified, the DC voltage established at the input terminal (G1) of the second amplifier (T2) is left at or brought to a value at which the second amplifier (T2) is unable to amplify the signals to be amplified.

8. The arrangement as claimed in one of claims 3 to 7, characterized in that when the DC voltage established at the input terminal (G1) of the first amplifier (T1) has a value at which the first amplifier (T1) is unable to amplify the signals to be amplified, the DC voltage established at the input terminal (G1) of the second amplifier (T2) is left at or brought to a value at which the second amplifier (T2) is able to amplify the signals to be amplified.

9. The arrangement as claimed in one of claims 3 to 8, characterized in that the DC voltage established at the input terminal (G1) of the first amplifier (T1) is adjustable or variable via the terminal (E1) via which the signals that are to be amplified by the first amplifier (T1) are fed to the arrangement.

10. The arrangement as claimed in one of the preceding claims, characterized in that the first and second amplifiers (T1, T2) are a first and a second transistor, and in that the conditions depending on which the second transistor is

operated are the level or the profile of the voltage established at the gate terminal of the first transistor.

11. The arrangement as claimed in one of claims 1 to 10, characterized in that the first and second amplifiers (T1, T2) are each designed as transistors with two gate terminals (G1, G2), of which the first gate terminal (G1) forms the terminal for the signal to be amplified and the second gate terminal (G2) forms the terminal for setting the gain, in that each of the amplifiers (T1, T2) is assigned a further transistor (H1, H2), with a controlled path and in each case two gate terminals, in that the gate terminals of the amplifiers (T1, T2) are respectively coupled to the gate terminals of the assigned further transistors (H1, H2), in that the controlled paths of the further transistors (H1, H2) are connected to the terminal for the ground potential (0) at one end and are coupled to the controlled path of the assigned amplifier (T1, T2) at the other end.

12. The arrangement as claimed in claim 11, characterized in that the terminals (G1) for a signal to be amplified of the amplifiers (T1, T2) are coupled to the gate terminals of the further transistors (H1, H2) in each case via the series circuit comprising two resistors (R_{E1a}, R_{E1b}, R_{E2a}, R_{E2b}), and in that the switched path of the switch (S1) and also a control terminal of the switch (S1) are in each case coupled to one of the nodes between the resistors (R_{E1a}, R_{E1b}, R_{E2a}, R_{E2b}) of in each case one of the series circuits.

Abstract

Arrangement having a first amplifier and a second amplifier, of which in each case only one at most is intended to effect amplification

The arrangement described is distinguished by the fact that the second amplifier (T2) is operated depending on the conditions established at the input terminal of the first amplifier (T1). As a result, it is possible to effect the changeover between the amplifiers with minimal outlay and without disturbing the amplifiers.

Figure